ARTICLE

The Impact of Dopant Segregation on the Maximum Carrier Density in Si:P Multilayers

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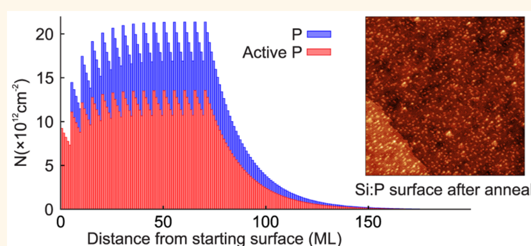
ABSTRACT Abrupt dopant profiles and low resistivity are highly sought after qualities in the silicon microelectronics industry and, more recently, in the development of an all epitaxial Si:P based quantum computer. If we increase the active carrier density in silicon to the point where the material becomes superconducting, while maintaining a low thermal budget, it will be possible to fabricate nanoscale superconducting devices using the highly successful technique of depassivation lithography. In this work, we investigate the dopant profile and activation in multiple high density Si:P δ-layers fabricated by stacking individual layers with intervening silicon growth. We determine that dopant activation is ultimately limited by the formation of P—P dimers due to the segregation of dopants between multilayers. By increasing the encapsulation thickness between subsequent layers, thereby minimizing the formation of these deactivating defects, we are able to achieve an active carrier density of $n_s = 4.5 \times 10^{14}$ cm^{-2} for a triple layer. The results of electrical characterization are combined with those of secondary ion mass spectroscopy to construct a model that accurately describes the impact of P segregation on the final active carrier density in Si:P multilayers. Our model predicts that a 3D active carrier density of 8.5×10^{20} cm^{-3} (1.7 atom %) can be achieved.



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Transistors beyond the 14 nm node will require electrically active dopant concentrations in excess of $\sim 10^{21}$ cm^{-3} to maintain performance, far beyond what is currently possible using traditional doping techniques such as ion implantation.[1] The use of two-dimensional doping methods has been suggested as a means to achieve higher active dopant concentrations in a range of materials for ultrashallow junctions,[2−4] avoiding the formation of deactivating dopant pairs in adjacent crystallographic planes. In particular, monolayer doping of Si has been used to produce high *n*-type sheet densities in silicon 2DEGs, reaching active carrier densities of (2−3) $\times$ 10^{14} cm^{-2} for both Sb and P dopants.[5,6] Recently, it has been demonstrated that an optimized double-dosing recipe yields a maximum active carrier density of $n_s = (3.6 \pm 0.1) \times 10^{14}$ cm^{-2} ($\sim$0.5 ML) in a single Si:P δ-layer without the formation of deactivating dopant precipitates.[7] To further increase the active carrier density, we propose the close stacking of multiple Si:P δ-layers with intervening silicon growth. Besides its application for the fabrication of ultrashallow junctions, this approach could potentially be used to achieve P concentrations beyond its solubility limit where theoretical studies predict superconducting behavior.[8] In the case of B doping, this has already been achieved for δ-doped layers using low-temperature molecular beam epitaxy ($n_s = 1 \times 10^{22}$ cm^{-3})[9,10] and more recently for a bulk structure using gas immersion laser doping ($n_s = 2.8 \times 10^{21}$ cm^{-3} (5.7 atom %)).[11] In the latter case, the boron-doped silicon was found to be superconducting. Together with surface depassivation lithography,[12] the low thermal budget approach of multiple atomic layer doping proposed here could provide a fabrication pathway for superconducting devices (*e.g.*, Josephson junctions, SQUIDs, and superconducting qubits) in silicon.[13] To this end, we investigate the active carrier density and shape of the P-profile in a triple Si:P layer fabricated by stacking individual δ-layers with intervening silicon growth. We show

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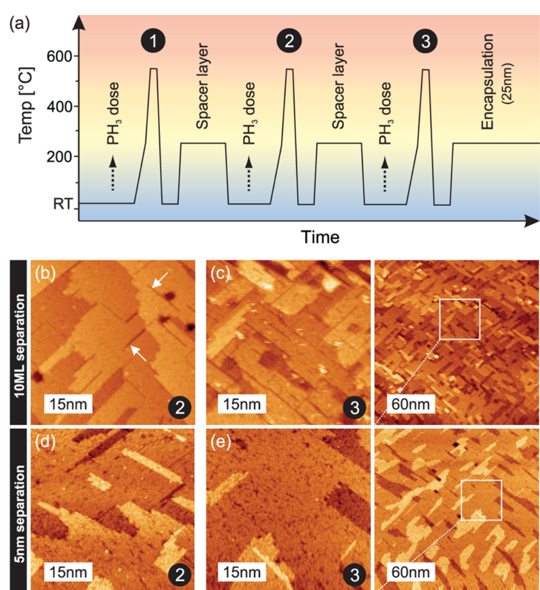

Figure 1. Formation of crystalline Si:P multilayers using a high temperature (550 °C) incorporation anneal. (a) Schematic of stacked multilayers growth using gaseous PH_3 doping of Si(001). High temperature anneals (550 °C, black circles) after each dose incorporate the P dopants, remove the H, and flatten the low temperature (250 °C) grown silicon spacer layers. STM images of the Si:P surface after the second and third incorporation anneals, respectively, for the case of a 10 ML (b and c) and 5 nm (d and e) thick spacer layer. Arrows in (b) mark two typical vacancy line defects.

that increasing the layer to layer separation increases the active carrier density and improves the epitaxial quality.

RESULTS AND DISCUSSION

Growth and Surface Characterization of Multilayers. The fabrication process and the temperature profile of the triple-layered samples are shown in Figure 1a. A single δ-layer grown under the same conditions as the triple layers presented in this work is known to produce an active carrier density of $n_s = (1.9 \pm 0.1) \times 10^{14}$ cm^{-2} with 100% activation.[14,15] Here, we focus our attention on the second and third δ-layer. Scanning tunneling microscopy (STM) images of the surface after the second and third incorporation anneal are shown in Figure 1b–e for the 10 ML and 5 nm thick spacer layer sample. We observe a low density of vacancy line defects on the surface of the 10 ML thick spacer layer sample after the second incorporation anneal, see white arrows in Figure 1b. These features are likely due to P present on the surface that has segregated from the previous P layer, leading to a combination of P–P and Si:P dimers forming on the surface. These segregated P atoms increase the surface strain which is relaxed by the formation of vacancy defects and, in turn, result in long chain dislocations.[16] The density of the vacancy line defects has increased in the third layer, see Figure 1c, suggesting a higher P–P density at this point in the structure. In the 5 nm thick spacer layer sample, the density of the vacancy line defects is significantly lower, see Figure 1d,e. The P segregation dynamics are the same in both samples, indicating that the thicker spacer layer helps to reduce the total amount of P present on the surface after the silicon growth, which leads to a reduction of line vacancy defects after incorporation of the second and third P layer. If we compare the larger overview images of the two samples after the third incorporation anneal, we find that the average uninterrupted terrace size is larger for the 5 nm thick spacer layer sample. This is a consequence of the decrease in number of line vacancy defects due to the recovery of the surface crystallinity for a thicker spacer layer. Note that, the vacancy line defects are not charged and will not be present in the bulk after overgrowth.

Modeling the P-Profile of Stacked Layers. Before we present the electrical transport results, we first introduce a model that estimates the P density profile in the triple layers. We can estimate the amount of P in the individual monolayers starting from the initial surface based on the probability p_{inc} for the dopant atoms to either incorporate into the Si surface or segregate to the growth interface.[17] The value is calculated from the expression $p_{inc} = a_0/4\Delta$, where Δ is the $1/e$ decay segregation length, recently measured as 2.4 nm for our system by high resolution atom probe tomography[18] and $a_0/4 = 0.1358$ nm, the distance between two subsequent Si(001) monolayers. For a single δ-layer, the number of dopant atoms that segregate to the surface n_{surf} is given by the expression:[17]

$$n_{surf} = n_{init}(1 - p_{inc})^N$$

where $n_{init} = 1.9 \times 10^{14}$ cm^{-2} is the initial amount of P dopants in the surface layer after dosing and incorporation,[14,15] and N is the number of monolayers of Si grown on top of the δ-doped layer. For our triple layer samples, we also have to consider the additional P atoms which have segregated to the growth front from previous dosings which reduces the amount of reactive Si available for additional P absorption. This is analog to the model presented in ref 7 where the number of available reactive sites was taken into account to describe the double-dosing recipe (*i.e.*, two sequential dosing and incorporation anneals). In the second and third layer, the starting value for the number of P dopants present on the growth front after dosing and incorporation is then given by

$$n^*_{init} = n^*_{surf} + \left(1 - \frac{n^*_{surf}}{n_{tot}}\right) n_{init}$$

where n^*_{surf} is the amount of P segregated to the surface before dosing and $n_{tot} = 6.8 \times 10^{14}$ cm^{-2} is the total number of atoms in a layer. This model gives us the P density as a function of the distance from the starting surface, see the blue profiles in Figure 2a,b. The red

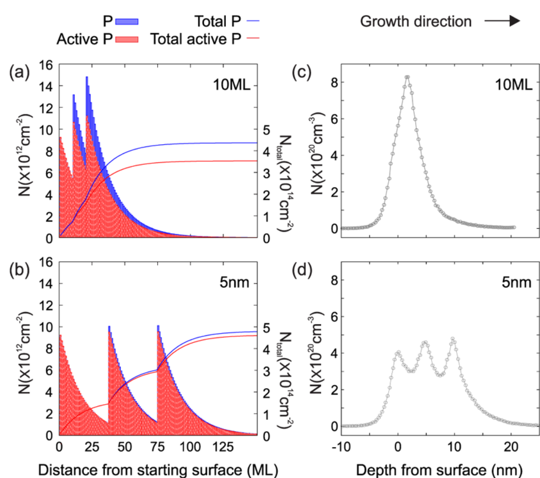

Figure 2. Estimated and measured dopant profiles of Si:P triple layers. (a) Segregation model for the 10 ML and (b) 5 nm thick spacer layers showing the estimated P (blue) and active P (red) sheet carrier density. Measured SIMS depth profile of (c) the 10 ML thick spacer layer sample showing a single thick doped region and (d) the 5 nm thick spacer layer sample where individual dopant layer peaks are resolved.

profiles in the graphs represent an extended segregation model which predicts the number of active P and will be introduced later. The total P present in the triple layer system can be obtained by integrating the density profiles and is given by the solid blue lines. The integration yields a maximum theoretical P sheet density for the total triple layer system of 4.4×10^{14} and 4.8×10^{14} cm^{-2} for the 10 ML and 5 nm thick spacer layer sample, respectively. It is important to note that the presence of P segregation in our model considerably lowers the maximum active carrier density that could be achieved by simply adding the maximum active carrier density of three single δ-layers (1.9×10^{14} cm$^{-2} \times 3 = 5.7 \times 10^{14}$ cm^{-2}). This highlights the significance of P present on the growth front as a factor that will limit further P incorporation and activation.

The P distribution calculations presented here however neglect the effects of diffusion of each layer which may also occur during each 550 °C incorporation anneal. To ascertain whether any substantial spreading occurred in these triple layers as a result of the incorporation anneals, we obtained SIMS analysis of each sample, shown in Figure 2, panels c and d for the 10 ML and 5 nm thick spacer layer samples, respectively. In the case of the 10 ML thick spacer layer, we cannot discern individual P peaks largely owing to the measurement resolution of SIMS (full width half-maximum of 1.3 nm)[19] and thus only observe a continuous thick δ-layer with a full width half-maximum of ~5 nm. In the 5 nm thick spacer layer sample, individual P peaks are discernible. These results match with the expected P distribution from the segregation calculations, thus demonstrating that minimal diffusion of P occurs during the 550 °C incorporation anneals.

TABLE 1. Results of the Magnetotransport Measurements[a]

d (ML)	n_s ($\times 10^{14}$cm^{-2})	σ_{xx} (Ω □$^{-1}$)	μ (cm^2/(V s))
5	3.2	457	42
10	3.6	373	46
20	4.1	287	52
37 (5 nm)	4.5	232	61

[a] The spacer layer thickness (d), active carrier density (n_s), zero-field resistivity $\sigma_{xx}(B = 0$ T), and mobility (μ) are listed.

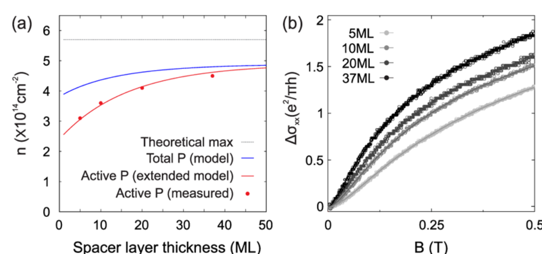

Figure 3. Comparison of modeling and electrical characterization of Si:P triple layers. (a) The expected total P concentration (blue line) plotted alongside the measured active carrier density (red circles) of triple layers with increasing interlayer spacing. The red line represents the active carrier density as predicted by our extended probability incorporation model. The theoretical maximum density possible for a Si:P triple layer (3× the value for a single δ-layer) is given by the dashed gray line. (b) The corrected conductivities $\Delta\sigma_{xx}(B)$ show a more pronounced two-dimensional weak localization feature as the thickness of the spacer layer increases. Fit to the Hikami model is superimposed on the data.

Electrical Characterization. The results of the magnetotransport measurements for 4 different samples with the interlayer separation changing from 5, 10, 20 to 37 ML (5 nm) are presented in Table 1. Compared to the well-established empirical relationship, which describes the mobility as a function of the active carrier density in bulk-doped silicon,[20] we find that the mobilities in our multilayers are ≈30% higher than what one would expect for equivalent active carrier densities in bulk. The measured active carrier density in all samples is substantially reduced from the overall maximum theoretical P density of 5.7×10^{14} cm^{-2} and decreases with decreasing spacer layer thickness. The downward trend is predicted by our probability incorporation model as shown in Figure 3a. Here, we show the experimentally obtained active carrier density (red dots) and the carrier density predicted by the model (blue line) *vs* the spacer layer thickness. We observe a discrepancy between the experimental results and the model, the former being much lower. Since the values of the parameters that govern the probability incorporation model (segregation length and initial P coverage) are well established and are proven for single δ-layers, the origin of the discrepancy has to be sought in the second and third dosing and incorporation anneal. The potential for P–P dimers to form during thin encapsulation layers can lower the active carrier density. From the STM images after the second

and third anneal, we know that the surface roughens as multiple layers are grown, see Figure 1b–e. The segregated P present at the growth front, combined with the relatively high thermal budget of the incorporation anneal (550 °C, 1 min), creates a favorable environment for substantial mass transport on/in the surface layer,[21] facilitating the formation of deactivating P–P dimers. We can readily incorporate the effect of this P–P dimer formation into our model by assuming that a fixed ratio of the P present in the surface layer, α, is deactivated by forming dimers with the newly deposited P during the incorporation anneal:

$$n^*_{init} = n^*_{surf} + \left(1 - \frac{n^*_{surf}}{n_{tot}}\right) n_{init} - 2\alpha n^*_{surf} \quad (3)$$

Note that this extended model now predicts the active P density where n^*_{surf} is still determined by the initial model that predicts the total P density. The value that yields the best fit with the measured active carrier density in all samples (see the red line in Figure 3a) is found to be α = 0.25, meaning that a quarter of the P already present on the surface will form a P–P dimer within a newly deposited layer. It is illustrative to plot the active carrier density profile predicted by our extended probability model alongside the profile of all the P present in the sample, see the red and blue shades regions in Figure 2a,b, respectively. We see that the active carrier density in the sample with the 10 ML thick spacer layer is severely affected due the large number of P present on the surface before the second and third dosing. In contrast, the two profiles in the case of the 5 nm thick spacer layer closely match. Here, the separation between the layers is large enough to suppress significant P segregation to the surface layer, increasing the number of available reactive sites for absorption and limiting P–P dimer formation during the incorporation anneal.

By looking at the magnetoconductivity of each of the samples in Figure 3b, we observe that as we increase the thickness of the overall dopant stack the 2D confinement as indicated by the sharpening of the weak localization dip around $B = 0$ T becomes more pronounced. This suggests that the electrical behavior of the 5 nm thick spacer layer sample corresponds to that of three noninteracting Si:P δ-layers despite some apparent overlap of dopant profiles from the SIMS measurements in Figure 2d. The closely spaced nature and intermixing of the P layers in the samples with the thinner spacing layers exhibits more bulk doped 3D behavior. Despited this, all the weak localization traces could be fitted to the Hikami model,[22] indicating that all samples can still be considered 2D. To achieve a truly 3D doping profile, a condition favorable for super conductivity in the Si:B material system, the number of layers in the sample has to been increased. Running our model for 20+ layers with a spacer layer thickness of 5 ML yields a 3D active carrier density of 9.1×10^{20} cm^{-3} (1.8 atom %). While still short of the density of 2.8×10^{21} cm^{-3} (5.7 atom %) at which superconductivity was observed in the Si:B material system, the P density might be increased further by combining the multilayer approach presented here with the double-dosing technique[7] and low temperature grown spacer layers to suppress P segregation.

CONCLUSIONS

To summarize, we find that we can increase the number of active P dopants in silicon by forming multilayers. An important challenge to achieving the maximum active carrier density in silicon is to minimize dopant segregation and P–P dimer formation during growth. The maximum active carrier density of 4.5×10^{14} cm^{-2} in a triple-layer sample was reached using a 5 nm thick spacer layer. Decreasing the spacer layer thickness resulted in a decrease of the active carrier density due to the presence of P on the growth surface. Not only does this reduce the number of active silicon sites available for further P absorption but leads to dopant deactivation by the formation of P–P dimers during the incorporation anneal. We developed a probability incorporation model to include these two effects which was found to accurately describe the active carrier density as a function of spacer layer thickness. Although the maximum carrier density reached (4.5×10^{14} cm^{-2}) is much higher than that of a single δ-layer (1.9×10^{14} cm^{-2}), it falls short of the theoretical maximum (5.7×10^{14} cm^{-2}). To further increase the active carrier density in multilayer systems and bring it closer to the theoretical maximum, dopant segregation has to be suppressed, either by increasing the growth rate or lowering the growth temperature of the spacer layers. Alternatively, we can use double dosing to increase the number of P in each layer. The current results improve the understanding of highly doped silicon superlattices to form ultra shallow junctions, for stacking of structured components for three-dimensional circuits, and the fabrication of super conducting Si:P.

METHODS

The samples discussed here were fabricated on (1–10) Ωcm Si wafers in an ultrahigh vacuum system with a 10^{-11} mbar base pressure. A clean Si(001)2 × 1 surface reconstruction was achieved by outgassing the sample for several hours at 450–470 °C, and subsequent heating to 1100 °C for 1 min. Monolayer doping was performed by self-saturating gaseous PH_3 doping of the Si surface at room temperature with an exposure of 1.35 Langmuir. This results in a 1 ML surface coverage of a combination of PH_2, PH, and H species with a total P coverage of ~0.37 ML.[14,23] An incorporation anneal of 550 °C is used to substitute P atoms into Si lattice sites and

remove the H species from the surface. During this process, a small amount of P and PH recombine to desorb as PH_2 reducing the overall surface coverage of P to ~0.25 ML.[14] A 550 °C incorporation temperature was chosen based on previous work on Si:P bilayers that demonstrated that the dopant activation of additional P layers is reliant upon achieving a flat Si surface due to thermal removal of H from the dissociated PH_x species.[15] A silicon sublimation cell produced epitaxial growth to encapsulate the dopants at 250 °C with an evaporation rate of ~1 ML min^{-1}. The thickness of the spacer layers separating the δ-layers was then varied from 5 ML to 5 nm. After the intervening Si growth, the process is repeated twice to achieve a total of three stacked multilayers. Finally, the total structure is capped with a 25 nm thick Si encapsulation layer. The whole dosing, incorporation, and growth recipe is summarized in Figure 1a. After the *in situ* formation of the triple Si:P layer, the samples were fabricated into Hall bars for electrical characterization. Secondary ion mass spectroscopy (SIMS) was used to characterize the shape of the P profiles in the growth direction after sample fabrication.

Conflict of Interest: The authors declare no competing financial interest.

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